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PATENT APPLICATION

METHOD OF FORMING BOTTOM OXIDE LAYER IN TRENCH STRUCTURE

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CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority from R.O.C. Patent Application No. 092102261, filed January 30, 2003, the entire disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a method of forming a bottom oxide layer, and more particularly to a method of forming a bottom oxide layer in a trench structure of a trench-type power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device.

[0003] Nowadays, trench-type power MOSFET devices are widely used in the semiconductor industry. During the manufacturing process for forming a trench-type power MOSFET, a bottom oxide layer is usually formed in a trench structure of a power MOSFET device to be served as a dielectric layer. For example, a conventional process for forming a bottom oxide layer in a trench structure of a trench-type power MOSFET device is described as follow. Figs. 1(a) to 1(c) are schematic cross-sectional views illustrating a conventional process for forming a bottom oxide layer in a trench structure of a trench-type power MOSFET device. As shown in Fig. 1(a), a pad oxide layer 11 and a silicon nitride layer 12 are sequentially formed on a semiconductor substrate 1. Then, the silicon nitride layer 12, the pad oxide layer 11, and the semiconductor substrate 1 are partially removed to form at least one trench structure 13 by the photolithography and etching process. Thereafter, as shown in Fig. 1(b), a silicon oxide layer 14 is formed on the silicon nitride layer 12 and on the bottom and sidewall of the trench structure 13 by the High Density Plasma Chemical Vapor Deposition (HDP-CVD) process. The thickness of the silicon oxide layer 14 formed by the HDP-CVD process is almost the same both on the bottom and sidewall. After the etching process is performed to remove the silicon oxide layer 14 on the sidewall of the trench structure 13, as shown in Fig. 1(c), only a portion of the silicon oxide layer 14 on the bottom of the trench structure 13 will remain and is defined as a bottom oxide layer 15.

[0004] However, the thickness of the bottom oxide layer typically is not enough after the above processes. In order to achieve the required thickness for the bottom oxide layer, the

HDP-CVD process and the etching process need to be repeated again and again. Due to the high cost of the HDP-CVD process and the need for repeated processes, the conventional method requires substantial cost and time to form a bottom oxide layer.

[0005] Another method for fabricating a concave bottom oxide in a trench structure is disclosed in U.S. Patent No. 6,265,269. The following is a summary of that method. First, as shown in Fig. 2(a), a semiconductor substrate 2 is provided, and a pad oxide layer 21 and a silicon nitride layer 22 are then sequentially formed on the semiconductor substrate 2. After that, the silicon nitride layer 22, the pad oxide layer 21, and the semiconductor substrate 2 are partially removed to form a trench structure 23 on the semiconductor substrate 2. Then, as shown in Fig. 2(b), a silicon oxide layer 24 is formed on the bottom and sidewall of the trench structure 23 and on the silicon nitride layer 22 by the Plasma Enhanced Chemical Vapor Deposition (PECVD) process, wherein the silicon oxide layer 24 has an overhang portion A at the corner of the trench structure 23. Subsequently, as shown in Fig. 2(c), an anisotropic etching process (i.e., the dry-etching process) is performed on the silicon oxide layer 24 to form a concave silicon oxide layer 24 in the trench structure 23 by using the overhang portion A as an etching mask to protect the silicon oxide layer 24 near the sidewall of the trench structure 23. Finally, as shown in Fig. 2(d), the wet-etching process is performed to remove the silicon oxide layer 24 on the sidewall of the trench structure 23 and on the silicon nitride layer 22 to form a bottom oxide layer 25 in the trench structure 23.

[0006] However, the anisotropic etching process and the dry-etching process both need to be used in the procedure of the above method, as shown in Figs. 2(c)~(d), and render the above method more complicated. Therefore, it is desirable to develop a method of forming a bottom oxide layer in a trench structure at reduced cost and time.

BRIEF SUMMARY OF THE INVENTION

[0007] Embodiments of the present invention are directed to a method of forming a bottom oxide in a trench structure applied to a trench-type power MOSFET device. The method according to the present invention not only can save the cost and time, but can also simplify the procedure steps.

[0008] In accordance with an aspect of the present invention, a method of forming a bottom oxide layer in a trench structure is provided. The method includes steps of (a) providing a semiconductor substrate and forming a trench structure on the semiconductor substrate; (b)

performing the plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source to deposit an oxide layer on the bottom and sidewall of the trench structure and the semiconductor substrate; and (c) removing the oxide layer on the sidewall of the trench structure substantially completely and the oxide layer on the bottom of the trench structure partially to define the remaining oxide layer as a bottom oxide layer.

[0009] In some embodiments, the step (a) further includes steps of: (a1) forming a pad oxide layer on the semiconductor substrate; (a2) forming a silicon nitride layer on the pad oxide layer; and (a3) removing the silicon nitride layer, the pad oxide layer and the semiconductor substrate partially to form a trench structure.

[0010] In specific embodiments, the step (a3) is performed by the photolithography and dry-etching process. The trench structure desirably has the aspect ratio between about 3.0 and about 4.0. The plasma-enhanced chemical vapor deposition (PECVD) process desirably is performed at a temperature of 440℃ to 520℃. The ratio of the thickness of the oxide layer deposited on the bottom of the trench structure to that on the sidewall of the trench structure is between about 1.5 and about 2.3. The step (c) may be performed by the wet-etching process. The etching selectivity of the oxide layer on the sidewall of the trench structure to that on the bottom of the trench structure is between about 2.5 and about 3. After the step (c), the steps of depositing and removing the oxide layer are repeated in sequence for allowing the bottom oxide layer to reach a required thickness. The oxide layer may be a silicon oxide layer.

[0011] In accordance with another aspect of the invention, a method of fabricating a trench-type power MOSFET comprises : (a) providing a semiconductor substrate and forming a trench structure on the semiconductor substrate; (b) performing the plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source to deposit an oxide layer on the bottom and sidewall of the trench structure and on the semiconductor substrate; (c) removing the oxide layer on the sidewall of the trench structure substantially completely and the oxide layer on the bottom of the trench structure partially to define the remaining oxide layer as a bottom oxide layer; and (d) forming a trench-type power MOSFET device in the trench structure.

[0012] In accordance with another aspect of the present invention, a method of forming a bottom oxide layer in a trench structure comprises providing a substrate having a trench

having a bottom and a sidewall; depositing an oxide layer on the bottom and sidewall of the trench by plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source at a temperature of about 440℃ to about 520℃; and removing the oxide layer on the sidewall of the trench substantially completely and the oxide layer on the bottom of the trench partially to form a remaining oxide layer as the bottom oxide layer on the bottom of the trench.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figs. 1(a) to 1(c) are schematic cross-sectional views illustrating a conventional process for forming a bottom oxide layer in a trench structure;

[0014] Figs. 2(a) to 2(d) are schematic cross-sectional views illustrating another conventional process for forming a bottom oxide in a trench structure; and

[0015] Figs. 3(a) to 3(d) are schematic cross-sectional views illustrating an exemplary embodiment of a process for forming a bottom oxide in a trench structure according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Embodiments of the present invention are directed to a method of forming a bottom oxide layer in a trench structure of a trench-type MOSFET device. Figs. 3(a) to 3 (d) are schematic cross-sectional views illustrating an exemplary embodiment process for forming a bottom oxide in a trench structure according to the present invention. As shown in Fig. 3(a), a semiconductor substrate 3, typically a silicon substrate, is provided. Then, a pad oxide layer 31 and a silicon nitride layer 32 are sequentially formed on the semiconductor substrate 3. Subsequently, the silicon nitride layer 32, the pad oxide layer 31 and the semiconductor substrate 3 are partially removed to form a trench structure 33 on the semiconductor substrate 3, for example, using a conventional photolithography and dry-etching process. The trench structure 33 is formed with the aspect ratio of typically between about 3.0 and about 4.0.

[0017] In Fig. 3(b), an oxide layer 34 is deposited on the bottom and the sidewall of the trench structure 33 and on the silicon nitride oxide layer 32. The oxide layer 34 may be formed by the plasma-enhanced chemical vapor deposition (PECVD) process with tetraethylorthosilicate (TEOS) as a gas source. By performing the PECVD-TEOS process at

a temperature of about 440℃ to about 520℃, preferably about 440℃ to about 480℃, the reaction speed of the molecules of the TEOS will be increased so as to have a ratio of the thickness of the oxide layer 34 deposited on the bottom (bt) of the trench structure 33 to that on the sidewall (sw) of the trench structure 33 between about 1.5 and about 2.3.

[0018] Thereafter, as shown in Fig. 3(c), the oxide layer 34 on the sidewall of the trench structure 33 is substantially completely removed and the oxide layer 34 on the bottom of the trench structure 33 is partially removed. The remaining oxide layer 34 on the bottom of the trench structure 33 is then defined as a bottom oxide layer 35. Usually, the bottom oxide layer 35 is used as a gate oxide layer of a trench-type MOSFET device. In this embodiment, the wet-etching process is performed to remove the oxide layer 34 on the sidewall of the trench structure 33 substantially completely and to leave the oxide layer 34 on the bottom of the trench structure 33 as much as possible. The wet-etching process is typically performed with a HF-based solution or a HF-based solution mixed with NHF solutes. Further, in the wet-etching process, the etching selectivity of the oxide layer 34 on the sidewall of the trench structure 33 to that on the bottom of the trench structure 33 is preferably between about 2.5 and about 3, thereby removing the oxide layer 34 on the sidewall of the trench structure 33 rapidly and leaving the oxide layer 34 on the bottom of the trench structure 33 as much as possible.

[0019] In addition, if the thickness of the bottom oxide layer 35 has not reached a required value after the above steps, as shown in Fig. 3(d), the deposition process and the etching process, i.e. the PECVD (plasma-enhanced chemical vapor deposition) process and the wet-etching process, are repeated until the bottom oxide layer 35 reaches the required thickness.

[0020] After the required thickness of the bottom oxide layer 35 on the trench structure 33 has been formed, subsequent processes are performed to form a trench-type power MOSFET in the trench structure 33.

[0021] To sum up, the present invention uses the PECVD-TEOS (i.e. plasma-enhanced chemical vapor deposition using TEOS as a gas source) process to form the oxide layer 34 at a temperature within a critical range of about 440℃ to about 520℃. Due to the high reaction temperature, TEOS molecules will be speeded up and the oxide layer 34 will be formed with a ratio of the thickness on the bottom of the trench structure 33 to that on the sidewall of the trench structure 33 between about 1.5 and about 2.3. Therefore, when the oxide layer 34 on the sidewall of the trench structure 33 is substantially completely removed, a portion of the

oxide layer 34 on the bottom of the trench structure 33 will remain and is defined as a bottom oxide layer. Accordingly, the less the oxide layer 34 on the bottom of the trench structure 33 is removed, the soon the required thickness of the bottom oxide layer 35 in the trench structure 33 is reached. Thus, the deposition process and the etching process need not be repeated again and again as before, and the cost and time are decreased accordingly.

[0022] Especially for a trench structure with high aspect ratio, the present invention can more easily control the thickness of the oxide layer 34 formed in the trench structure 33 than other conventional processes. Further, the oxide layer 34 formed by the PECVD-TEOS process is free from the generation of any particle and has better electrical characteristics.

[0023] Moreover, by using a the wet-etching process with the high etching selectivity of the oxide layer on the sidewall of the trench structure 33 to that on the bottom of the trench structure 33, the oxide layer 34 on the sidewall of the trench structure 33 can also be removed substantially completely in a short time and a much greater portion of the oxide layer 34 remains on the bottom of the trench structure 33 than before when conventional processes are used. In addition, the conventional HDP-CVD process is limited by equipment and requires a higher cost. The methods according to embodiments of the present invention avoid these problems. Therefore, the present invention not only saves cost and time, but also allows the thickness of the bottom oxide layer to be controlled more easily.

[0024] The above-described arrangements of apparatus and methods are merely illustrative of applications of the principles of this invention and many other embodiments and modifications may be made without departing from the spirit and scope of the invention as defined in the claims. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.